Fraunhofer IIS

DAC8b6GS055nm

8 Bit 6 GS/s Current Steering DAC

Key Parameters

- Resolution: 8 bit
- Conversion rate: 4 to 6 GS/s
- Power consumption: < 350 mW
- Signal-to-Noise: > 43 dB (up to 3 GHz)
- Spurious-free dynamic range: > 46 dB (up to 3 GHz)
- Differential output voltage: +/- 800 mV (100 Ω load)
- Supply voltage core: 1.2 V +/- 5 %
- Supply voltage peri: 3.3 V +/- 5 %
- Operating clock: 4 to 6 GHz
- Temperature range: - 40 °C to 125 °C

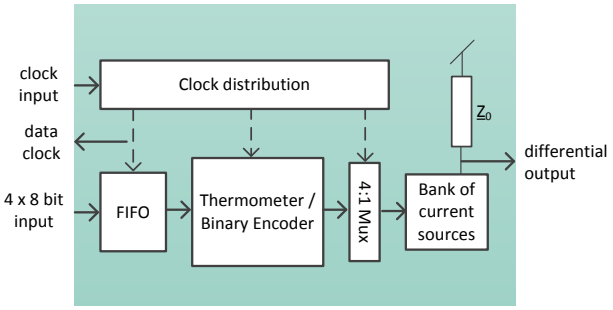

Fig. 1: IP-Level Block Diagram

General Description

The IP consists of an 8 bit current steering DAC clocked externally for 4 - 6 GS/s.

The **differential output signal** of maximum +/- 800 mV is driven onto a load impedance of 100 Ohm and can be calibrated within a range of +/- 25 % of its nominal value to adjust to load conditions.

The IP needs an **external clock** with high accuracy and low periodic jitter, because the clock jitter influences the dynamic behavior of the converter.

The digital input word of 8 bits is taken as a 4x parallel bus. A data clock provides the frequency; phase sync for the data interface is done via an internal FIFO.

The DAC is **silicon evaluated** in **Fujitsu 55 nm CS250L** technology.

Fraunhofer IIS provides a **detailed documentation** and **support** for the IP integration.
Modifications, extensions and technology ports of the IP are available on request.

Benefits

- Low design risk due to silicon evaluated design
- Robust operation across full temperature range from - 40 °C up to 125 °C
- Tunability of full-range voltage provides adaptable amplitude while keeping full resolution

Deliverables

- GDSII data
- Simulation model
- Documentation
- Integration support

FACT SHEET

CONTACT

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